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Attached please find an English translation for KR 2001-0037699, which was applied in a rejection of Paper No. 20060915.

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Korean Laid-Open Patent
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METHOD FOR FORMING CAPACITOR

Yu-Jin Lee

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METHOD FOR FORMING CAPACITOR

[Kopaesito hyungsong bangbeop]

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Applicant:	Hyundai Electronics Ind. Co., Ltd.

[There are no amendments to this patent.]

Specification

Brief description of the figures

Figure 1 is a sequential cross section showing a conventional method for forming a capacitor.

Figure 2 is a sequential cross section showing an application example of the present invention.

Explanation of numerals of the main parts of the invention

10 Semiconductor substrate
20 First oxide film
30 Cell plug
40 Bit-line electroconductive film
50 Bit line cap
60 Bit line sidewall

70 Second oxide film
80 First nitride film
90 Third nitride film
100 Storage node contact
110 Second nitride film
120 Fourth oxide film
130 Polysilicon
140 Spin-on glass
150 Dielectric substance
160 Upper electrode of capacitor

Detailed explanation of the invention

Purpose of the invention

Technical field of the invention and prior art of the field

The present invention pertains to a method for forming a capacitor. In particular, the present invention pertains to a method for forming a capacitor that can extend the surface area without raising an oxide film which determines the height of a capacitor in a semiconductor memory manufacturing process, so that the aspect ratio in the above-mentioned oxide film etching is not increased and the capacitance is appropriately increased.

The conventional method for forming a capacitor is explained referring to the sequential cross sections of Figures 1a-1c.

The conventional method consists of a contact and anti-etching film formation process that constitutes a bit line by sequentially forming first oxide film (2), cell plug (3), bit-line electroconductive film (4), bit line cap (5), and bit line sidewall (6) on a semiconductor substrate (1) on which a MOS transistor is formed, forms a second oxide film (7) on it, forms a storage node contact (8) to be connected to the above-mentioned cell plug (3), and vapor-deposits a nitride film (9) on the structure; a capacitor lower-electrode formation process that vapor-deposits a third oxide film (10) on the entire surface of the above-mentioned formed structure, vapor-deposits a hole by dry-etching the third oxide film (10) and the nitride film (9), vapor-deposits a polysilicon (11) on the structure, fills the above-mentioned formed hole by spreading a spin-on glass (12) on it, and etches it back; and a capacitor upper-electrode formation process that etches the polysilicon (11) exposed due to the above-mentioned etch back, removes the spin-on glass (12), removes the third oxide film (10) of the lower electrode of the capacitor exposed in the above-mentioned process by dry-etching, and sequentially vapor-deposits a dielectric substance (13) and an upper electrode (14) of the capacitor on the entire surface of the above-mentioned structure.

First, as shown in Figure 1a, the first oxide film (2) is vapor-deposited onto the semiconductor substrate (1), dry-etched so that a source/drain region (S/D) of the above-mentioned formed MOS transistor can be exposed, and polysilicon is vapor-deposited onto it and flattened, so that the cell plug (3) is formed.

The bit line electroconductive film (4) and the bit line cap (5) are sequentially vapor-deposited onto the entire surface of the above-mentioned formed structure, dry-etched to fit to a region where a bit line is formed, and the bit line sidewall (6) is formed on the side surface of the structure of the above-mentioned formed bit-line electroconductive film (4) and bit line cap (5) by using an insulating film, so that the bit line is constituted.

The second oxide film (7) is formed on the above-mentioned formed structure, and a storage node contact hole is formed by dry-etching the above-mentioned vapor-deposited second oxide film (7) so that it can be connected to the above-mentioned cell plug (3). Then, polysilicon is vapor-deposited onto the structure and flattened, so that the storage node contact (8) is formed. Then, the nitride film (9) is vapor-deposited onto it and the second oxide film (7) and used as an anti-etching film. At that time, the above-mentioned structure becomes a memory cell except for the capacitor.

Next, as shown in Figure 1b, the third oxide film (10) is vapor-deposited onto the entire surface of the above-mentioned formed structure, and a hole is formed by dry-etching the third oxide film (10) and the nitride film (9) so that the above-mentioned storage node contact (8) can be exposed. Then, the polysilicon (11) is vapor-deposited onto the structure, and the above-mentioned formed hole is filled by spreading the spin-on glass (12) on it and etched back until the polysilicon (11) is exposed, so that a lower electrode of the capacitor is formed. The spin-on glass (12) in the above-mentioned etch back process is overetched, so that part of the upper part of the above-mentioned formed hole is not filled.

Next, as shown in Figure 1c, if the polysilicon (11) exposed by the above-mentioned etch back is etched, the polysilicon (11) positioned on the above-mentioned structure is removed up to the position of the spin-on glass (12), the spin-on glass (12) is removed by dry-etching, the third oxide film (10) in the lower electrode of the capacitor exposed in the process for removing the above-mentioned polysilicon (11) is removed by dry-etching, and the dielectric substance (13) and the upper electrode (14) of the capacitor are sequentially vapor-deposited onto the entire surface of the above-mentioned structure.

Technical problems to be solved by the invention

However, in the above-mentioned conventional method for forming capacity, since the part enclosed with the storage node contact, the lower electrode of the capacity, and the bit line cap was wasted and the method for raising the lower electrode of the capacitor by raising the

vapor-deposition height of the third oxide film was utilized to increase the capacitance of the capacitor, if etching was applied to it, the aspect ratio was increased, so that the subsequent processes were difficult.

The present invention has been created to solve the above-mentioned conventional problems, and the objective of the present invention is to provide a method for forming a capacitor that can increase the capacity of a capacitor without raising a third oxide film by using a part enclosed with a storage node contact, a capacity lower-electrode, and a bit line cap, so that if the lower electrode of the capacity is formed by etching it, the aspect ratio can be regulated, thereby enabling increase of the capacitance of the capacitor by an easy process.

Constitution and operation of the invention

In order to achieve the above-mentioned objective, the method for forming a capacitor of the present invention is characterized by consisting of a contact and anti-etching film formation process that constitutes a bit line by sequentially forming first oxide film, cell plug, bit-line electroconductive film, bit line cap, and bit line sidewall on a semiconductor substrate on which a MOS transistor is formed, sequentially forms second oxide film, first nitride film, and third oxide film on it, forms a storage node contact to be connect to the above-mentioned cell plug, and vapor-deposits a second nitride film on the structure; a capacitor lower-electrode formation process that vapor-deposits a fourth oxide film forms a hole by dry-etching the fourth oxide film and the second nitride film so that the above-mentioned storage node contact can be exposed, vapor-deposits polysilicon on the above-mentioned structure, fills the above-mentioned formed hole by spreading a spin-on glass onto it, and etches it back; and a capacity expansion and upper electrode formation process that removes the spin-on glass after etching the polysilicon exposed by the above-mentioned etch back, removes the fourth oxide film and its lower second oxide film in the capacitor lower-electrode exposed in the above-mentioned process by dry-etching them, expands the surface area of the lower electrode of the capacitor by wet-etching the third oxide film exposed through the above-mentioned process, and sequentially vapor-deposits the dielectric substance and the upper electrode of the capacitor on the entire surface of the above-mentioned structure.

The above-mentioned method for forming a capacity of the present invention is explained as follows in detail by using sequential cross sections of the attached Figures 2a-2c.

First, as shown in Figure 2a, a first oxide film (20) is vapor-deposited onto a semiconductor substrate (10) on which a MOS transistor is formed an then dry-etched so that a source/drain region (S/D1) of the above-mentioned formed MOS transistor can be exposed, and polysilicon is vapor-deposited onto it and flattened, so that a cell plug (30) is formed.

A bit-line electroconductive film (40) and a bit line cap (50) are sequentially vapor-deposited onto the entire surface of the above-mentioned formed structure, dry-etched to fit to a region where a bit line is formed, and a bit line sidewall (60) is formed on the side surface of the structure of the above-mentioned formed bit-line electroconductive film (40) and bit line cap (50) by using an insulating film, so that a bit line is constituted.

Second oxide film (70), first nitride film (80), and third oxide film (90) are sequentially formed on the above-mentioned formed structure, and a storage node contact hole is formed by dry-etching the above-mentioned vapor-deposited insulating films (90, 80, 70) so that it can be connected to the above-mentioned cell plug (30). Then, polysilicon is vapor-deposited onto the structure and flattened, so that a storage node contact (100) is formed. Then, a second nitride film (110) is vapor-deposited onto it and the third oxide film (90) and used as an anti-etching film. At that time, the above-mentioned structure becomes a memory cell except for the capacitor.

Next, as shown in Figure 2b, a fourth oxide film (120) is vapor-deposited onto the entire surface of the above-mentioned formed structure, and a hole is formed by dry-etching the fourth oxide film (120) and the second nitride film (110) so that the above-mentioned storage node contact (100) can be exposed, and a polysilicon (130) is vapor-deposited onto it. Then, the above-mentioned formed hole is filled by spreading a spin-on glass (140) on it and etched back until the polysilicon (130) is exposed, so that a lower electrode of the capacitor is formed. The spin-on glass (140) in the above-mentioned etch back process is overetched, so that part of the upper part of the above-mentioned formed hole is not filled.

Next, as shown in Figure 2c, if the polysilicon (130) exposed by the above-mentioned etch back is etched, the polysilicon (130) positioned on the above-mentioned structure is removed up to the position where the spin-on glass (140) exists, the spin-on glass (140) is removed by dry-etching, the fourth oxide film (120) and its lower second nitride film (110) in the lower electrode of the capacitor exposed in the process for removing the above-mentioned polysilicon (130) are removed by dry-etching, and the third oxide film (90) exposed through the above-mentioned process is wet-etched, so that the surface area of the lower electrode of the capacitor is expanded. Then, a dielectric substance (150) and an upper electrode (160) of the capacitor are sequentially vapor-deposited onto the entire surface of the above-mentioned structure.

Effects of the invention

As mentioned above, according to the method for forming a capacitor of the present invention, with the use of the part enclosed with the storage node contact, the lower electrode of the capacitor, and the bit line cap, which has not bee used in the prior art, as a lower electrode,

the capacitance of the capacitor can be regulated by combining the height of the third oxide film and the fourth oxide film, so that even if the capacitor capacitance is raised, the etching aspect ratio is not increased. Thereby, the product production is made easy, and the quality can be improved.

Claim

A method for forming a capacitor, characterized by consisting of a contact and anti-etching film formation process that constitutes a bit line by sequentially forming first oxide film, cell plug, bit-line electroconductive film, bit line cap, and bit line sidewall on a semiconductor substrate on which a MOS transistor is formed, sequentially forms second oxide film, first nitride film, and third oxide film on it, forms a storage node contact to be connect to the above-mentioned cell plug, and vapor-deposits a second nitride film onto the structure; a capacitor lower-electrode formation process that vapor-deposits a fourth oxide film forms a hole by dry-etching the fourth oxide film and the second nitride film so that the above-mentioned storage node contact can be exposed, vapor-deposits polysilicon on the above-mentioned structure, fills the above-mentioned formed hole by spreading a spin-on glass on it, and etches it back; and a capacity expansion and upper electrode formation process that removes the spun-on glass after etching the polysilicon exposed by the above-mentioned etch back, removes the fourth oxide film and its lower second oxide film in the capacitor lower-electrode exposed in the above-mentioned process by dry-etching them, expands the surface area of the lower electrode of the capacitor by wet-etching the third oxide film exposed through the above-mentioned process, and sequentially vapor-deposits the dielectric substance and the upper electrode of the capacitor on the entire surface of the above-mentioned structure.

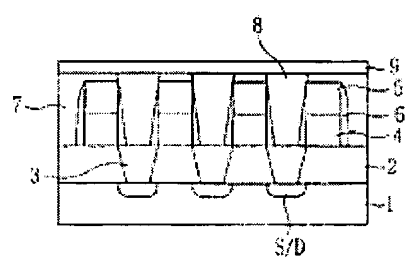

Figure 1a

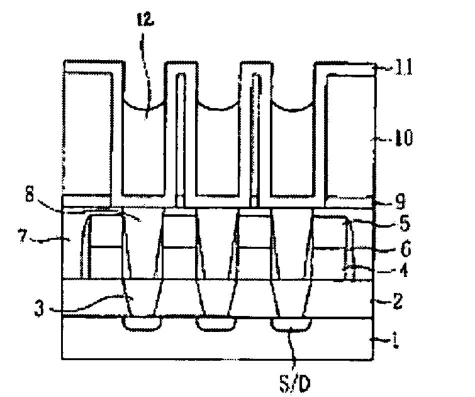

Figure 1b

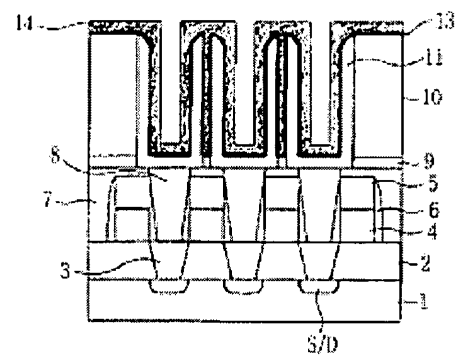

Figure 1c

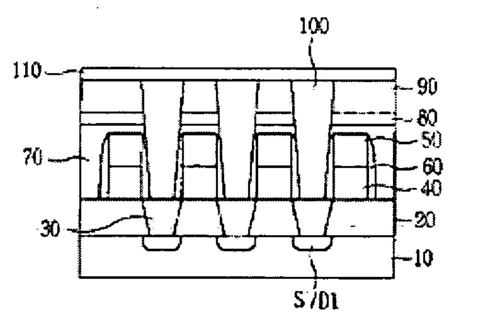

Figure 2a

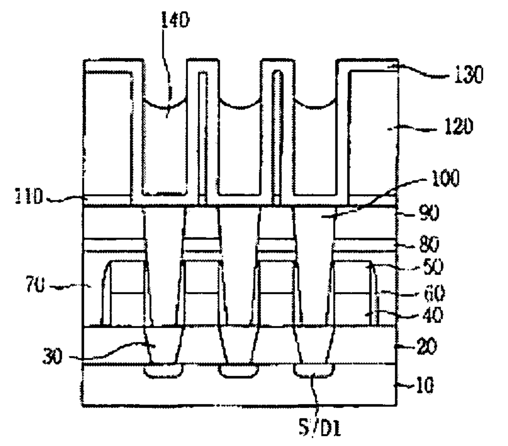

Figure 2b

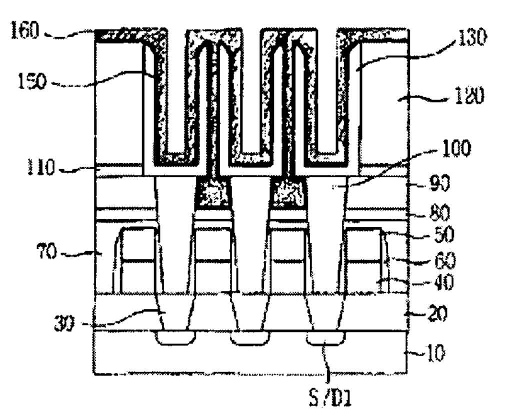

Figure 2c